

Listing of Claims

Claims 1-12 have been cancelled.

13. **(Presently Amended)** A memory back-up system comprising:
 a volatile memory cell;
 a non-volatile memory cell, the non-volatile memory cell being integrated with the volatile memory cell, the non-volatile memory cell being interfaced with the volatile memory cell;
 a single word line WL [common control line] connected to the integrated volatile memory cell and the non-volatile memory cell, the single word line WL [common control line] allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell.
14. **(Original)** The memory back-up system of claim 13, wherein the volatile memory cell is a DRAM memory cell and the non-volatile memory cell is an MRAM memory cell.
15. **(Presently amended)** The memory back-up system of claim 13, further comprising a second control line which in combination with the single word line WL [common control line] provides selection of the volatile memory cell.
16. **(Presently amended)** The memory back-up system of claim 13, further comprising a third control line which in combination with the single word line WL [common control line] provides selection of the non-volatile memory cell.
17. **(Presently Amended)** The memory back-up system of claim 13, further comprising a
 an array volatile memory cells;

an array of non-volatile memory cells, each non-volatile memory cell interfaced with a corresponding volatile memory cell;

a plurality of word lines WL [common control lines], each single word line WL [common control line] connected to a corresponding plurality of volatile memory cells and the non-volatile memory cells, the word line WL [common control line] allowing data to be simultaneously written to the corresponding plurality of volatile memory cells and the non-volatile memory cells.

18. **(Previously Cancelled)** A memory back-up system comprising:

a plurality of first memory cells;

a plurality of non-volatile memory cells that are interfaced to the first memory cells;

control circuitry that allows data to be written to one of the first memory cells and the non-volatile memory cells, and that provides transfer of the data from one of the first memory cells and the non-volatile memory cells to the other one of the first memory cells and the non-volatile memory cells.

19. **(Previously Cancelled)** The memory back-up system of claim 18, wherein the control circuitry further includes allowing data to be read from one of the first memory cell and the non-volatile memory cell.

20. **(Presently Amended)** A computing device comprising:

a controller;

a memory unit interfaced with the controller, the memory unit comprising;

an array volatile memory cells;

an array of non-volatile memory cells, each non-volatile memory cell integrated and interfaced with a corresponding volatile memory cell; and

a plurality of word lines WL [common control lines], each word line WL [common control line] connected to a corresponding plurality of the integrated volatile memory cells and the non-volatile memory cells, the word line WL [common control line] allowing data to be simultaneously written to the corresponding plurality of volatile memory cells and the non-volatile memory cells.

21. **(Presently Amended)** An image storing device comprising:
means for receiving an image;
a memory unit for storing the image, the memory unit comprising;
an array volatile memory cells;
an array of non-volatile memory cells, each non-volatile memory cell integrated and interfaced with a corresponding volatile memory cell; and
a plurality of word lines WL [common control lines], each word line WL [common control line] connected to a corresponding plurality of the integrated volatile memory cells and the non-volatile memory cells, the word line WL [common control line] allowing data to be simultaneously written to the corresponding plurality of volatile memory cells and the non-volatile memory cells.

22. **(Presently Amended)** The memory back-up system of claim [11] 21, further comprising a plurality word lines, wherein a single word line WL is connected to both [the] a first memory cell and [the] a non-volatile memory cell.

23. **(Previously added)** The memory back-up system of claim 22, wherein the single word line WL is connected to a DRAM controlling transistor gate of the DRAM memory cell and a to a MRAM controlling transistor gate of the MRAM memory cell.

24. **(Presently amended)** A memory back-up system comprising:
a volatile memory cell;

a non-volatile memory cell that is interfaced with the volatile memory cell;

a single word line WL [common control line] connected to the volatile memory cell and the non-volatile memory cell, the single word line WL [common control line] allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell; wherein

the volatile memory cell is a DRAM memory cell and the non-volatile memory cell is an MRAM memory cell.